CLAIMS

What is claimed is:

1. A digital signal processor comprising:

a policy statement table for storing a plurality of policy statements; and

a priority index table for storing a plurality of priority numbers, each priority number associated with a corresponding policy statement and indicating the priority of the corresponding policy statement relative to the other policy statements.

2. The digital signal processor of claim 1, wherein the policy statement table comprises a content addressable memory (CAM).

3. The digital signal processor of claim 3, wherein the CAM comprises a ternary CAM.

4. The digital signal processor of claim 1, wherein the priority index table comprises priority logic coupled to the policy statement table.

5. The digital signal processor of claim 4, wherein the priority logic to provide to a plurality of signal lines an indication of a location of the most significant priority number in the priority index table.

6. The digital signal processor of claim 5, further comprising a memory array coupled to the plurality of signal lines and for storing routing information for the policy statements, the indication to select routing information from the memory array for one of the policy statements.

7. The digital signal processor of claim 5, further comprising an encoder having inputs coupled to the plurality of signal lines to receive the indication.

8. The digital signal processor of claim 4, wherein the most significant priority number is the priority number with the smallest numerical value.

9. The digital signal processor of claim 4, wherein the most significant priority number is the priority number with the largest numerical value.

10. The digital signal processor of claim 4, wherein the priority logic provides the most significant priority number to a plurality of priority signal lines.

11. The digital signal processor of claim 10, wherein the priority logic comprises:

a plurality of compare circuits each coupled to one of the plurality of priority signal lines and the policy statement table; and

a plurality of isolation circuits each coupled to one of the plurality of priority signal lines and one of the plurality of compare circuits.

12. The digital signal processor of claim 11, wherein the priority logic further comprises means for determining whether to compare at least two priority numbers already stored in the priority index table, or to compare the priority numbers stored in the priority index table with a priority number not stored in the priority index table.

13. The digital signal processor of claim 1, further comprising an instruction decoder coupled to the policy statement table and the priority index table.

14. The digital signal processor of claim 1, further comprising decrement logic coupled to the policy index table.

15. The digital signal processor of claim 1, further comprising increment logic coupled to the policy index table.

16. The digital signal processor of claim 1, further comprising flag logic coupled to the policy statement table, the flag logic to generate a flag signal indicating when one policy statements matches a policy search key.

17. The digital signal processor of claim 1, further comprising cascade logic coupled to the priority index table and having inputs to receive a priority number from another digital signal processor, the cascade logic for outputting from the digital signal processor a priority number from the priority index table or the priority number from the another digital signal processor.

18. A digital signal processor comprising:

a content addressable memory (CAM) array having a plurality of rows of CAM cells; and

a first array of storage elements coupled to the CAM array, each row of storage elements for storing a number corresponding to a data word stored in one of the rows of the CAM cells.

19. The digital signal processor of claim 18, wherein the rows of CAM cells are for storing policy statements, and the numbers comprise priority numbers of the policy statements, a priority number indicating the priority of a corresponding policy statement relative to the other policy statements.

20. The digital signal processor of claim 18, wherein the rows of CAM cells are for storing Internet Protocol (IP) addresses, and the numbers comprise prefix mask data for the IP addresses.

21. The digital signal processor of claim 18, further comprising priority logic coupled to the first array of storage elements, the priority logic to provide to a

plurality of signal lines an indication of a location of a particular number in the first array of storage elements.

22. The digital signal processor of claim 21, wherein the plurality of signal lines is coupled to the CAM array.

23. The digital signal processor of claim 21, further comprising a second array of storage elements, each row of the second array coupled to one of the plurality of signal lines to receive the indication, the indication to select one of the rows of the second array.

24. The digital signal processor of claim 21, further comprising an encoder having inputs coupled to the plurality of signal lines to receive the indication, and having a plurality of outputs to provide an encoded address of the location of the number in the first array of storage elements.

25. The digital signal processor of claim 24, wherein the encoded address corresponds to an address in the CAM array of the data word that corresponds with the number stored at the indicated location in the first array of storage elements.

26. The digital signal processor of claim 24, further comprising a decoder coupled to the CAM array, and wherein the plurality of outputs of the encoder are coupled to the decoder.

27. The digital signal processor of claim 24, further comprising a second array of storage elements, each row of the second array coupled to one of the plurality of outputs of the encoder.

28. The digital signal processor of claim 19, further comprising a plurality of priority signal lines each coupled to one of the storage elements in each row of the first array.

29. The digital signal processor of claim 28, wherein the priority logic comprises:

a first plurality of compare circuits, each compare circuit coupled to one of the storage elements in the first array of storage elements, and each compare circuit having a first input coupled to a storage element, a second input coupled to a match line, and an input/output line coupled to one of the plurality of priority signal lines; and

an isolation circuit, the isolation circuit associated with the most significant bit of the each number having an input coupled to the match line, and an output, each additional isolation circuit associated with the other bits of each number having an output, and an input coupled to the output of the previous higher order bit.

30. The digital signal processor of claim 29, wherein each row of storage elements in the first array is configured to form a counter.

31. The digital signal processor of claim 30, further comprising a second plurality of compare circuits each coupled to one of the counters, and each having a first plurality of inputs to receive a first number stored in the respective counter, a second plurality of inputs each coupled to one of the plurality of priority signal lines to receive a second number provided thereon, and an output coupled to the counter, each of the second compare circuits providing a control signal on its output to indicate whether to update the first number stored in the respective counter.

32. The digital signal processor of claim 31, wherein each of the second plurality of compare circuits determines when the first number is greater than or equal to the second number.

33. The digital signal processor of claim 31, wherein each of the second plurality of compare circuits determines when the first number is less than or equal to the second number.

34. The digital signal processor of claim 28, wherein each row of storage elements in the first array is configured to form a counter.

35. The digital signal processor of claim 34, further comprising a plurality of compare circuits each coupled to one of the counters, and each having a first plurality of inputs to receive a first number stored in the respective counter, a second plurality of inputs each coupled to receive a second number, and an output coupled to the counter, each of the second compare circuits providing a control signal on its output to indicate whether to update the first number stored in the respective counter.

36. The digital signal processor of claim 35, wherein each of the plurality of compare circuits determines when the first number is greater than or equal to the second number.

37. The digital signal processor of claim 35, wherein each of the second plurality of compare circuits determines when the first number is less than or equal to the second number.

38. The digital signal processor of claim 18, further comprising priority logic having inputs coupled to the first array of storage elements, and outputs to

provide the most significant number from a selection of numbers in the first array.

39. The digital signal processor of claim 38, wherein the first array comprises a second CAM array having a plurality of match lines, and wherein the outputs of the priority logic are coupled to the second CAM array.

40. The digital signal processor of claim 39, wherein the second CAM array compares the most significant number with the numbers stored in its array and asserts its plurality of match lines in response to the comparison.

41. A digital signal processor comprising:

a content addressable memory (CAM) array for storing a plurality of data words and determining that a search key matches more than one of the data words;

first storage means for storing a plurality of numbers, each number corresponding to a data word in the CAM array; and

means for determining a location in the second storage means of a most significant number associated with one of the data words that matches the search key.

42. The digital signal processor of claim 41, further comprising means for generating an address of the location in the first storage means.

43. The digital signal processor of claim 42, further comprising second storage means for storing another plurality of data words, one of which is accessed in response to the address of the location in the first storage means.

44. The digital signal processor of claim 41, further comprising means for accessing the data word in the CAM array that corresponds to the most significant number.

45. The digital signal processor of claim 41, further comprising means for determining the most significant number.

46. The digital signal processor of claim 45, wherein the most significant number is the largest numerical number.

47. The digital signal processor of claim 45, wherein the most significant number is the lowest numerical number.

48. The digital signal processor of claim 41, further comprising means for determining that at least one of the numbers stored in the first storage means is greater than or equal to an external number not stored in the first storage means.

49. The digital signal processor of claim 48, further comprising means for updating the at least one number that is greater than or equal to the external number.

50. The digital signal processor of claim 49, further comprising means for writing the external number to the first storage means.

51. The digital signal processor of claim 41, further comprising means for determining that at least one of the numbers stored in the first storage means is less than or equal to an external number not stored in the first storage means.

52. The digital signal processor of claim 51, further comprising means for updating the at least one number that is less than or equal to the external number.

53. The digital signal processor of claim 52, further comprising means for writing the external number to the first storage means.

54. The digital signal processor of claim 41, wherein the CAM array comprises a ternary CAM array having data storage cells for storing the plurality of data words, and further having mask storage cells for storing mask data on a bit-for-bit basis for the data words.

55. The digital signal processor of claim 54, wherein the data words comprise policy statements, and the numbers comprise priority numbers for the policy statements.

56. The digital signal processor of claim 54, wherein the data words comprise Internet Protocol (IP) addresses, and the numbers comprise prefix mask data.

57. A method of operating a digital signal processor, comprising:

determining that a search key matches more than one of a plurality of data words stored in a first memory; and

determining a location in a second memory of a most significant number associated with the data words that match the search key.

58. The method of claim 57, further comprising generating an address of the location in the second memory.

59. The method of claim 58, further comprising accessing a location in a third memory in response to the address of the location in the second memory.

60. The method of claim 57, further comprising accessing a location in a third memory in response to determining the location in the second memory.

61. The method of claim 60, wherein the data processor is incorporated into a router, the data words comprise policy statements, and the most significant number is the most significant priority number, wherein each policy statement has a priority number that indicates the priority of the corresponding policy statement relative to other policy statements in a given policy.

62. The method of claim 57, further comprising determining the most significant number.

63. The method of 62, wherein the most significant number is the number with the largest numerical value.

64. The method of claim 62, wherein the most significant number is the number with the highest numerical value.

65. A method of adding a new policy statement to a plurality of policy statements stored in a first memory, comprising:

comparing a new priority number associated with the new policy statement to a plurality of priority numbers stored in a second memory, the plurality of priority numbers each associated with a respective one of the plurality of policy statements stored in the first memory;

determining that the new priority number is more significant than one of the plurality of priority numbers stored in the second memory;

updating the determined priority number in the second memory without changing its physical location in the second memory;

writing the new priority number to an available location in the second memory; and

writing the new policy statement to an available location in the first memory.

66. The method of claim 65, wherein the new priority number is more significant than the determined priority number when the new priority number is greater than or equal to the determined priority number.

67. The method of claim 65, wherein the new priority number is more significant than the determined priority number when the new priority number is less than or equal to the determined priority number.

68. A method of adding a new policy statement to a plurality of policy statements stored in a first memory, comprising:

altering a new priority number associated with the new policy statement;

comparing the altered new priority number to a plurality of priority numbers stored in a second memory, the plurality of priority numbers each associated with a respective one of the plurality of policy statements stored in the first memory;

determining that the altered new priority number is more significant than one of the plurality of priority numbers stored in the second memory;

updating the determined priority number in the second memory without changing its physical location in the second memory;

writing the unaltered new priority number to an available location in the second memory; and

writing the new policy statement to an available location in the first memory.

69. The method of claim 68, wherein the altered new priority number is more significant than the determined priority number when the altered new priority number is greater than the determined priority number.

70. The method of claim 68, wherein the altered new priority number is more significant than the determined priority number when the altered new priority number is less than the determined priority number.

71. The method of claim 68, wherein altering the new priority number comprises decrementing the new priority number.

72. The method of claim 68, wherein altering the new priority number comprises incrementing the new priority number.

73. A method of deleting a policy statement from a plurality of policy statements stored in a first memory, comprising:

comparing a priority number associated with the policy statement to a plurality of priority numbers stored in a second memory, the plurality of priority numbers each associated with a respective one of the plurality of policy statements stored in the first memory;

determining that the priority number is equal to one of the plurality of priority numbers;

providing an indication of the location of the matched priority number in the second memory to the first memory to access the policy statement; and

deleting the policy statement from the first memory.

74. The method of claim 73, further comprising:

comparing the priority number with the plurality of priority numbers in the second memory;

determining that the priority number is less than one of the plurality of priority numbers;

updating the determined priority number without changing its physical location in the second memory, and without changing the physical location in the first memory of the policy statement associated with the determined priority number.

75. The method of claim 73, further comprising:

comparing the priority number with the plurality of priority numbers in the second memory;

determining that the priority number is greater than one of the plurality of priority numbers;

updating the determined priority number without changing its physical location in the second memory, and without changing the physical location in the first memory of the policy statement associated with the determined priority number.

76. A system comprising:

a first digital signal processor comprising:

a first content addressable memory (CAM) array for storing a first plurality of data word and determining that a search key matches more than one of the first data words;

first storage means for storing a first plurality of numbers, each number corresponding to a data word in the first CAM array;

means for determining a first most significant number associated with one of the first data words that matches the search key; and

outputs for providing the first most significant number; and

a second digital signal processor comprising:

a second CAM array for storing a second plurality of data words and determining that the search key matches more than one of the second data words;

second storage means for storing a second plurality of numbers, each number corresponding to a data word in the second CAM array;

means for determining a second most significant number associated with one of the second data words that matches the search key;

first inputs coupled to the outputs of the first digital signal processor; and

cascade logic coupled to the first inputs and the second storage means, the cascade logic to compare the first most significant number with the second most significant number.

77. The system of claim 76, wherein the cascade logic outputs the more significant number between the first and second most significant numbers.

78. The system of claim 77, wherein the more significant number is the number that has the largest numerical value.

79. The digital signal processor of claim 77, wherein the more significant number is the number that has the smallest numerical value.

80. The system of claim 76, further comprising a third digital signal processor comprising:

a third content addressable memory (CAM) array for storing a third plurality of data word and determining that the search key matches more than one of the third data words;

third storage means for storing a third plurality of numbers, each number corresponding to a data word in the third CAM array;

means for determining a third most significant number associated with one of the third data words that matches the search key; and

outputs for providing the third most significant number; and wherein the second digital signal processor further comprises second inputs coupled to the outputs of the third digital signal processor, and wherein the cascade logic is coupled to the second inputs to compare the second most significant number with the third most significant number.

81. The system of claim 80, wherein the cascade logic outputs the more significant number between the first and second most significant numbers.

82. The system of claim 81, wherein the more significant number is the number that has the largest numerical value.

83. The digital signal processor of claim 82, wherein the more significant number is the number that has the smallest numerical value.

84. The digital signal processor of claim 76, wherein the data words comprise policy statements, and the numbers comprise priority numbers for the policy statements.

85. The digital signal processor of claim 76, wherein the data words comprise Internet Protocol (IP) addresses, and the numbers comprise prefix mask data.

86. A priority circuit for determining the most significant number from binary numbers stored in separate rows of memory cells in a memory array, and for identifying the row in which the most significant number is stored, comprising:

a plurality of priority signal lines each coupled to one of the memory cells of each of row of the array; and

a plurality of priority logic circuits each coupled to one of the memory cells, and each having a first input, a second input coupled to one of the memory cells, an input/output (I/O) coupled to one of the plurality of priority signal lines, and an output, wherein within one row of the memory array, each priority logic circuit has its output connected to the input of the next successive priority logic circuit.

87. The priority circuit of claim 86, wherein the plurality of priority logic circuits each comprise:

a compare circuit coupled to the first input, second input, and I/O line of the priority logic circuit; and

an isolation circuit coupled to the first input and the output of the priority logic circuit.